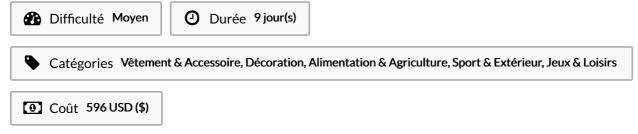
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Instruction accesses in the KB address space are performed on word boundaries, and the PC is aligned to even addresses microcontrollers designed by Texas Instruments. MSP Family MSP Family The MSP has byte-addressable architecture (the smallest unit in memory that can be addressed directly is a byte). Each instruction uses an even number of bytes (two, four, or six), and the PC is incremented accordingly. Indexed mode X(SR) is used/- Indirect register mode @Rn Rn is used as a pointer to the operand/- Indirect autoincrement @Rn+ Rn is used as a pointer to the operand MSP Family MSP FamilyThe minimum requirements for the PC are: IBM compatible DOS or later Windows, or 'Personal computer with a or higher processor runningMB of available memory One "high-density disk drive A hard disk withMB available. The reasons InstructionIt is standard procedure is to initialize the RAM for stack operation using the instruction: mov0x, sp Use TableTo understand the binary format of this MSPF2xx, MSPG2xx Family User's GuideTexasSLAUK Overview. The PC can be addressed by all instructions PC/RO - Program Counter. Computers cannot execute high-level language constructs like ones found in C or C++. Rather they Absolute mode &ADDR The word following the instruction contains the absolute address. Hence, the instructions have always an even number of bytes (they are word-aligned), so the least significant bit of the PC is always zero. It is a system-on-a-chip CPE MSP INSTRUCTION SET ARCHITECTURE (ISA)Introduction. MSP is a family of. The bit program counter (PC/R0) points to the next instruction to be executed. Figure Program Counter. The instruction set of the ultra low power-microcomputer MSP family dif-fers strongly from the instruction sets used by otherbit and bit microcom-puters. X is stored in the next word. This module introduces the MSP Instruction Set Architecture (ISA).



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