

# Synopsys spyglass cdc user guide pdf

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It describes how to set up the design environment for CDC analysis, perform CDC checks using VC SpyGlass, and debug any CDC violations found. VC SpyGlass CDC provides an easy-to-use and comprehensive guide for solving CDC problems at the RTL and gate-level netlist to avoid costly re-spins. Every single flop will get reported by SpyGlass as one of the following: Synchronized. Methodology documentation and rule-tags integrated for direct use User-guided CDC methodology results in fewer, more meaningful violations, saving time for the RTL designer Highest performance and CDC/RDC centric debug capabilities. Low learning curve and ease of adoption CDC Methodology GuideSpyGlass Console User Guide SpyGlass Console Reference Guide GuideWareEarly Adopter GuideWare GuideWare Number Number of of inverters/buffers inverters/buffers between between sync sync flops flops exceeds exceeds limit limit (Control) (Control) Using SpyGlass to Resolve Unsync'd. Unsyncronized This document provides a user guide for VC SpyGlass Clock Domain Crossing (CDC) analysis. Key features of VC SpyGlass CDC include integrity checks, synchronization checks, convergence checks, and glitch checks to verify correct data transfer between Methodology CDC Methodology Guide Constraints Methodology Guide Design Read-In Methodology Guide DFT Methodology Guide DFT-DSM Methodology GuideTXV Methodology Missing: synopsys This course will focus on clock domain crossings challenges and how you can identify and fix them using VC SpyGlass CDC. This will help designers to catch the silicon failure SpyGlass\_CDCMethodology\_GuideWare\_UserGuideFree download as PDF File.pdf), Text File.txt) or read online for g: synopsys VC\_SpyGlass\_CDC\_Quick\_Start\_GuideFree download as PDF File.pdf), Text File.txt) or read online for g: synopsysVC SpyGlass CDC provides an easy-to-use and comprehensive guide for solving CDC problems at the RTL and gate-level netlist to avoid costly re-spins. Hierarchical SoC flow to support IP based design methodologies to deliver quickest turnaround time for very large size SoCs. Integrated with other SpyGlass solutions for RTL signoff for lint, constraints, DFT and power.

 Difficulté Difficile

 Durée 968 heure(s)

 Catégories Énergie, Machines & Outils, Sport & Extérieur

 Coût 55 USD (\$)

## Sommaire

Étape 1 -  
Commentaires

Matériaux

Outils

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Étape 1 -

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