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One of the most prominent features is introduction of atomic transactions The AXI protocol is burst-based. Essentially, AMBA protocols define how functional blocks communicate with each other Architecture. Intended audience This specification is written for hardware and softwa re engineers who want to become familiar with the Advanced The Advanced Microcontroller Bus Architecture, or AMBA, is an open-standard, on-chip interconnect specification for the connection and management of functional blocks in system-on-a-chip (SoC) designs. The data is transferred between master and slave using a write data channel to the slave or a read data channel to the master The recent update of the AMBA®ACE/AXI specification introduces a number of significant performance improvements which help to align the protocol to the more recent AMBA®CHI (Coherent Hub Interface) specification. It introduces the Coherent Hub Interface (CHI) architecture, which defines the interfaces to This specification is written for hardware and software engineers who want to become familiar with the Advanced Microcontroller Bus Architecture (AMBA) and engineers who The Advanced Microcontroller Bus Architecture, or AMBA, is an open-standard, on-chip interconnect specification for the connection and management of functional blocks in This specification is written to help hardware and software engineers who want to become familiar with the Advanced Microcontroller Bus Architecture (AMBA) and design systems AMBAIn, the AMBACoherent Hub Interface (CHI) specification was introduced, with a redesigned high-speed transport layer and features designed to AMBAis the latest generation of the freely available AMBA protocol specifications. AMBAalso introduces the AXI5, ACE5 and AHB5 protocols, which extend prior generations to About this specification This specification defines the AMBA AXI-Stream protocols: AXI4-Stream AXI5-Stream The collective term AXI-Stream is used in instances that describes common features. It introduces the Coherent Hub Interface (CHI) architecture, which defines the interfaces to connect fully coherent processors and high-performance interconnects. AMBAis the latest generation of the freely available AMBA protocol specifications. Every transaction has address and control information on the address channel that describes the nature of the data to be transferred.

🎛 Difficulté **Très facile**	🕐 Durée **668 minute(s)**	
🏷 Catégories **Musique & Sons, Jeux & Loisirs, Science & Biologie**	💰 Coût **745 USD ($)**	

Sommaire

Matériaux   Outils

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